CLAIMS

What is claimed:

1. An apparatus for sampling an input signal, wherein the apparatus receives a clock signal synchronous with the input signal, the apparatus comprising:
   a. a synthesizer for receiving the synchronous clock signal, wherein the synthesizer produces a synthesized signal having a synthesized signal frequency dependent on the synchronous clock signal; and
   b. a sampling module coupled to the synthesizer, wherein the sampling module samples the input signal based on the synthesized signal frequency.

2. The apparatus according to claim 1 further comprising a counter coupled to the synthesizer and the sampling module, wherein the counter sends a strobe signal to the sampling module after a predetermined amount of counts.

3. The apparatus according to claim 1 further comprising a processing unit coupled to the sampling module, wherein the processing unit analyzes a sampled point from the sampling module and arranges the sampled point in an eye diagram.

4. The apparatus according to claim 3 wherein the synthesizer signal frequency is programmed as the function

$$F_{DDS} = \frac{1}{R} \bullet \left(\frac{N}{N+1} \right) F_{CLK}$$

wherein R is an integer, N is an amount of sample points per unit interval and F_{CLK} is the clock frequency.

5. The apparatus according to claim 4 wherein the eye diagram is formed by arranging an x-coordinate of a particular sample point using the function:

$$x(i) = \mathrm{mod}(R \bullet C \bullet i, N)$$

wherein C is the predetermined number of counts and i is the particular sample point.

6. The apparatus according to claim 1 further comprising a processing unit coupled to the synthesizer, wherein the processing unit controls the synthesizer signal frequency.

7. The apparatus according to claim 2 further comprising a processing unit coupled to the counter, wherein the processing unit controls the predetermined number of counts.

8. The apparatus according to claim 1 further comprising a prescaler module coupled to the synthesizer and the synchronous clock signal, wherein the prescaler module adjusts the synchronous clock signal to an acceptable clock frequency to be input into the synthesizer.

9. An apparatus for analyzing an input signal, wherein the apparatus receives a clock signal having a clock frequency synchronous with the input signal, the apparatus comprising:

a. a synthesizer for receiving the clock signal, wherein the synthesizer produces a signal having a synthesizer frequency dependent on the clock frequency;

b. a counter coupled to the synthesizer, the counter for receiving the signal and producing a strobe signal;

c. a sampling module coupled to the counter, the sampling module for sampling the input signal upon receiving the strobe signal; and

d. a processor coupled to the sampling module, wherein the processor analyzes a sample point from the sampling module and arranges the sample point in a desired configuration.

10. The apparatus according to claim 9 wherein the desired configuration is an eye diagram.

11. The apparatus according to claim 9 wherein the processing unit controls the synthesizer frequency.

12. The apparatus according to claim 9 wherein the counter produces the strobe signal after a predetermined number of counts.

13. The apparatus according to claim 12 wherein the sampling module samples the input signal at a sampling frequency, wherein the sampling frequency is dependent on the synthesizer frequency and the predetermined number of counts.

14. The apparatus according to claim 9 wherein the processing unit controls the predetermined number of counts.

15. The apparatus according to claim 9 further comprising a prescaler module coupled to the synthesizer and the clock signal, wherein the prescaler module adjusts the clock frequency to an acceptable level to be input into the synthesizer.

16. A method of analyzing an input signal comprising:

a. receiving a clock signal synchronous with the input signal;

b. generating a synthesized signal from the clock signal, wherein the synthesized signal has a synthesized signal frequency; and

c. sampling the input signal dependent on the synthesized signal frequency.

17. The method according to claim 16 further comprising adjusting the clock signal to an acceptable clock frequency to generate the synthesized signal.

18. The method according to claim 17 wherein the input signal is sampled at a sampling point after a predetermined number of counts, C.

19. The method according to claim 18 wherein the synthesized signal frequency is a function:

$$F_{DDS} = \frac{1}{R} \bullet \left(\frac{N}{N+1} \right) F_{CLK}$$

wherein R is an integer and N is a number of sample points per unit interval.

20. The method according to claim 19 further comprising arranging an i^{th} sampling point to form an eye diagram with a horizontal resolution of N points per unit interval using function:

$$\mathbf{x(i) = mod(R \bullet C \bullet \mathit{i}, N)}$$

21. A method of analyzing deterministic jitter of a repetitive input signal having a length of L bits, the method comprising:

a. receiving a clock signal synchronous with the input signal;

b. generating a synthesized signal from the clock signal;

c. sampling the input signal at a plurality of sample points, wherein the input signal is sampled dependent on a synthesized signal frequency;

d. adjusting a phase of the synthesized signal frequency such that the plurality of sample points are located on one or more edges of the input signal;

e. calculating a bit edge value for each sample point in the plurality;

f. averaging the sample points; and

g. calculating a deterministic jitter component.

22. The method according to claim 21 further comprising adjusting the clock signal to an acceptable clock frequency to generate the synthesized signal.

23. The method according to claim 22 wherein the input signal is sampled at each sample point after a predetermined number of counts, C.

24. The method according to claim 23 wherein the synthesized signal frequency is a function:

$$F_{DDS} = \frac{1}{R} \bullet F_{CLK}$$

25. The method according to claim 24 wherein the bit edge index is arranged for an i^{th} sample point using function:

$$B(i) = \mathbf{mod}(R \bullet C \bullet i, L)$$

26. The method according to claim 25 wherein the deterministic jitter component is duty cycle distortion jitter.

27. The method according to claim 25 wherein the deterministic jitter component is intersymbolic interference jitter.